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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/620,679
Filing Date: July 20, 2000
Appellant(s): RUESCH, RODNEY

David W. Black
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/25/2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existance of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 7-16 and 23-25 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,337,254	KNEE et al.	9-1994
6,118,310	ESCH, Jr.	9-2000

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 7 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Knee et al. (US 5,337,254).

3. With respect to claim 7, figures 1-4 of Knee teaches a method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal (100);

adjusting a first resistance (activating transistor 1X connected to VDD at 110, figure 3) coupled to a first supply voltage (VDD), based on a manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 70, figure 1);

adjusting a second resistance (activating another transistor 1X connected to ground at 110, figure 3) coupled to a second supply voltage (ground), based on the manufacturing process, the first supply voltage and the temperature (PVT control signal from 18 through microprocessor to 70); and

adjusting a third resistance (activating another transistor 2X connected to ground at 112, figure 1) coupled to the second supply voltage (ground), based on the manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 72).

4. With respect to claim 23, figure 3 of Knee teaches adjusting a first resistance (1X of 110) includes changing a resistance of a semiconductor.

5. With respect to claim 24, figure 3 of Knee teaches adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).

6. With respect to claim 25, figure 1 of Knee teaches selecting a predetermined number of programmable bits from a plurality of programmable bits (microprocessor provides bits (inputs to 70, 72, 74) to 16 to control the resistance.)

7. Claims 8-10, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Esch, Jr. (US 6,118,310).

8. With respect to claim 8, figures 4-6 of Esch teaches a method of communicating data in an integrated circuit using internal interconnections, the method comprising:

selecting a resistance of a divider network (select resistor based on 262, 264 of figure 6) based on a manufacturing process, a supply voltage and a temperature;

selecting an edge rate of a driver (edge rate is controlled by 266) coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal (203); and

providing an output (output at 241) based on the data signal, the resistance, and the edge rate.

9. With respect to claim 9, figure 6 of Esch teaches selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

10. With respect to claim 10, figure 5 of Esch teaches providing an output turning on a PFET transistor (212) and turning off an NFET transistor (222).

11. With respect to claim 15, figure 5 of Esch discloses the step of receiving a tristate enable signal (ENABLE); and actuating a switchable resistance element (230) in response to the tristate enable signal.

12. With respect to claim 16, figure 5 of Esch discloses actuating a switchable resistance element comprises actuating a programmable inverter (230 configured as inverter).

Allowable Subject Matter

13. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance:

With respect to claim 11, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

With respect to claim 12, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

With respect to claim 11, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting an edge rate of a driver coupled to a divider network comprises programming for selecting resistance elements from a parallel resistance elements.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

(11) Response to Argument

(A) The rejection of Claims 7 and 23-25 Under 35 U.S.C. 102(b)

Appellant argues that "ground supply voltage" is oxymoronic and cannot properly be construed as " a second supply voltage." This argument is incorrect in that the prior art and appellant's disclosure show a logic circuit must include a power rail. This power rail goes from one potential (e.g. VSS) to a second potential (VTT is higher than VSS) in order for the circuit to function. VSS is usually 0 Volt. However, it is still considered to be a particular potential. Zero volt is still higher that a negative voltage. Applicant's disclosure (figures 1-13) shows the first

potential is VTT and the second potential is VSS (ground) and does disclose any other second potential.

(B) The rejection of Claims 8 and 10 under 35 U.S.C. 102(e)

Appellant argues that the prior art (Esch) does not teach any steps of the claimed method.

Guidance in response to this argument is found in the MPEP section 2112.01 as follows:

> MPEP section 2112.01 Composition, Product and Apparatus Claims
> **PRODUCT AND APPARATUS CLAIMS — WHEN THE STRUCTURE RECITED IN THE REFERENCE IS SUBSTANTIALLY IDENTICAL TO THAT OF THE CLAIMS, CLAIMED PROPERTIES OR FUNCTIONS ARE PRESUMED TO BE INHERENT**
> Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

The Esch prior art used under 35 U.S.C. 102(e) is clearly in alignment with MPEP section 2112.01 and addressing the inherency of providing a method claim with an apparatus.

With respect to claim 8, figures 4-6 of Esch teaches a method of communicating data in an integrated circuit using internal interconnections, the method comprising:

selecting a resistance of a divider network (select resistor based on 262, 264 of figure 6) based on a manufacturing process, a supply voltage and a temperature

(see abstract, the circuit compensate for Process, Variation, and temperature (PVT));

selecting an edge rate of a driver (edge rate is controlled by 266) coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal (203); and

providing an output (output at 241) based on the data signal, the resistance, and the edge rate (edge rate is control by turning on particular transistors 211-229 in figure 5).

With respect to claim 9 argument, appellant stated that the prior art does not provide "word for word" of maintaining a substantially constant edge rate. This feature is inherent in the apparatus of Esch in that the output signal at pad 241 in figure 4 is maintained at a constant edge by turning particular transistors 211-229 for variation of PVT. Otherwise, the output signal will be distorted due to environment conditions.

With respect to claim 15, applicant argues that Esch does not teach, "Receiving a tristate enable signal and actuating resistance element in response to the tristate enable signal." Figure 5 of Esch shows an enable signal (ENABLE) controlling a switchable resistance element 230. Therefore, the claimed element is anticipated.

With respect to claim 16, applicant argues that Esch does not teach actuating a programmable inverter. Figure 5 of Esch shows the output of the switching element 230 is an inverted output based on the enable signal. When the enable signal is high logic level, the output of 230 is low logic level and when the enable signal is low logic level the output of 230 is high logic level. Therefore, the switchable element is a programmable inverter.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Don Le
November 20, 2002

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